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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,198	11/21/2003	Gregory E. Howard	TI-29600.1	2992

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,198	HOWARD ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *12-13* is/are allowed.

6)☐ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date NO
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 120 claiming priority from parent U.S. Application No. 10/020604 filed on December 14, 2001 which itself claims priority from provisional Application No. 60/257,708 filed on December 22, 2000 .

Continued Prosecution Application

The request filed on 11/21/2003 for a Divisional Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 10/020604 is acceptable and a Divisional has been established. An action on the Divisional follows.

Information Disclosure Statement

There are no IDS filed to date in this Application.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment filed 11 /21 /2003.

Therefore claims 1-13 as recited in the preliminary amendment are currently pending in the Application.

Claims 14- 20 have been cancelled by the preliminary amendment.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,970,352 (herein after Shiozawa) in view of U.S. Patent No. 5231,038 (herein after Yamamguchi).

With respect to claim 1 Shiozawa describes a method for constructing a semiconductor device, the method comprising: forming a trench isolation structure (Shiozawa fig. 3 a # 117, col. 3 line 67) and an active region proximate an outer surface of a semiconductor layer; (Shiozawa fig. 3 a # 113 etc., col.4 line 2) depositing an epitaxial layer outwardly from the trench isolation structure, (Shiozawa fig. 3b # 141, col. Col.5 line 11) growing a first insulator layer outwardly from the epitaxial layer; (Shiwozawa fig. 3 b #127) growing a second insulator layer outwardly from the first insulator layer; (Shiozawa col. 4 lines 54-55) forming a gate stack outwardly from the epitaxial layer, the gate stack comprising a portion of the first insulator layer, a portion of the second insulator layer, and a gate formed proximate the second insulator layer, (Shiozawa fig. 3a-b # 125a-c).

Shiozawa does not specifically describe a gate having a narrow region and a wide region.

However, Yamaguchi in fig. 1 J # 52 and col.9 lines 1-3 describes a gate electrode having a narrow region and a wide region, so that a filed effect transistor producing method that can be used to from optimum thickness gate insulating film and the side-wall insulating film independently of each other, thus ensuring a device with least dielectric breakdown.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Yamaguchi's a gate electrode having a narrow region and a wide region in Shiozawa's method steps . The motivation to include the above substitution is so that a filed effect transistor producing method that can be used to from optimum thickness gate insulating film and the side-wall insulating film independently of each other, thus ensuring a device with least dielectric breakdown. (col. 6 lines 50-66 and 15-20).

The remaining limitations of claim1 are :

and heating the epitaxial layer to a temperature sufficient to allow for the epitaxial layer to form a source/drain implant region in the active region. (Shiozawa figure #I, col. 6 lines30-37).

With respect to claim 2 Shiozawa describes the method of Claim 1, wherein the trench isolation structure comprises silicon dioxide. (Shiozawa col.4 lines 33-35).

With respect to claim 3 Shiozawa describes the method of Claim 1, wherein the epitaxial layer has a thickness of approximately 1,000 angstroms to 3,000 angstroms. (Shiozawa col. 5 line 11-12).

With respect to claim 4 Shiozawa describes the method of Claim 1, wherein the epitaxial layer comprises silicon. (Shiozawa col. 5 line 23).

With respect to claim 5 Shiozawa describes the method of Claim 1, wherein the epitaxial layer comprises silicon germanium. (Shiozawa col. 4 lines 25-30).

With respect to claim 6 Shiozawa describes wherein the epitaxial layer comprises silicon germanium carbon. (Shiozawa col.4 lines 25-30).

With respect to claim 7 Shiozawa describes the method of Claim 1, wherein the first insulator layer comprises silicon dioxide. (Shiozawa col.4 lines 39-41).

With respect to Claim 8 Shiozawa describes the method of Claim 1, wherein the second insulator layer comprises silicon nitride. (Shiozawa col. 4 lines 63-65).

With respect to claim 9 Shiozawa describes the method of Claim 1, wherein the gate stack comprises a third insulator layer formed outwardly from the second insulator layer, the third insulator layer comprising silicon dioxide. (Shiozawa col. 4 line 62-65).

With respect to Claim 10 Shiozawa describes the method of Claim 1, wherein forming the gate stack comprises etching the second insulator layer; etching the first insulator layer to form a gate region; growing a gate insulator layer outwardly from the gate region', and forming the gate outwardly from the gate insulator layer. (Shiozawa 3a-f).

With respect to Claim 11 Shiozawa describes the method of Claim 1, wherein forming the gate stack comprises: etching the second insulator layer using a dry etching process', etching the first insulator layer using a wet etching process to form a gate

region; growing a gate insulator layer outwardly from the gate region; and forming the gate outwardly from the gate insulator layer. (Shiozawa fig.s 3a –f and Yamaguchi col. 8 line 27-28-dry etching).

.Allowable Subject Matter

Claims 12 and 13 allowed.

The following is a statement of reasons for the indication of allowable subject matter:

The following is an examiner's statement of reasons for allowance:

The prior art taken either singularly or in combination fails to anticipate or fairly suggest the limitation of the dependent claims, in such manner that a rejection under 35 U.S.C. 102 or 103 would be proper. The prior art fails to teach a combination of all the claimed features as presented in independent claims, which include a gate as recited in claims 1-11 including having a length of the narrow region of the gate is approximately one-tenth microns to two microns', and a width of the narrow region of the gate is approximately 25 microns to 100 microns (claim 12) or wherein a length of the wide region of the gate is approximately two-tenths microns to two microns greater than a length of the narrow region of the gate. (claim 13) . (see also parent case USP 6,680,504).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718 The examiner can normally be reached on 8.00 to 5.00.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao

Patent examiner

July 23, 2004

SPE 2814